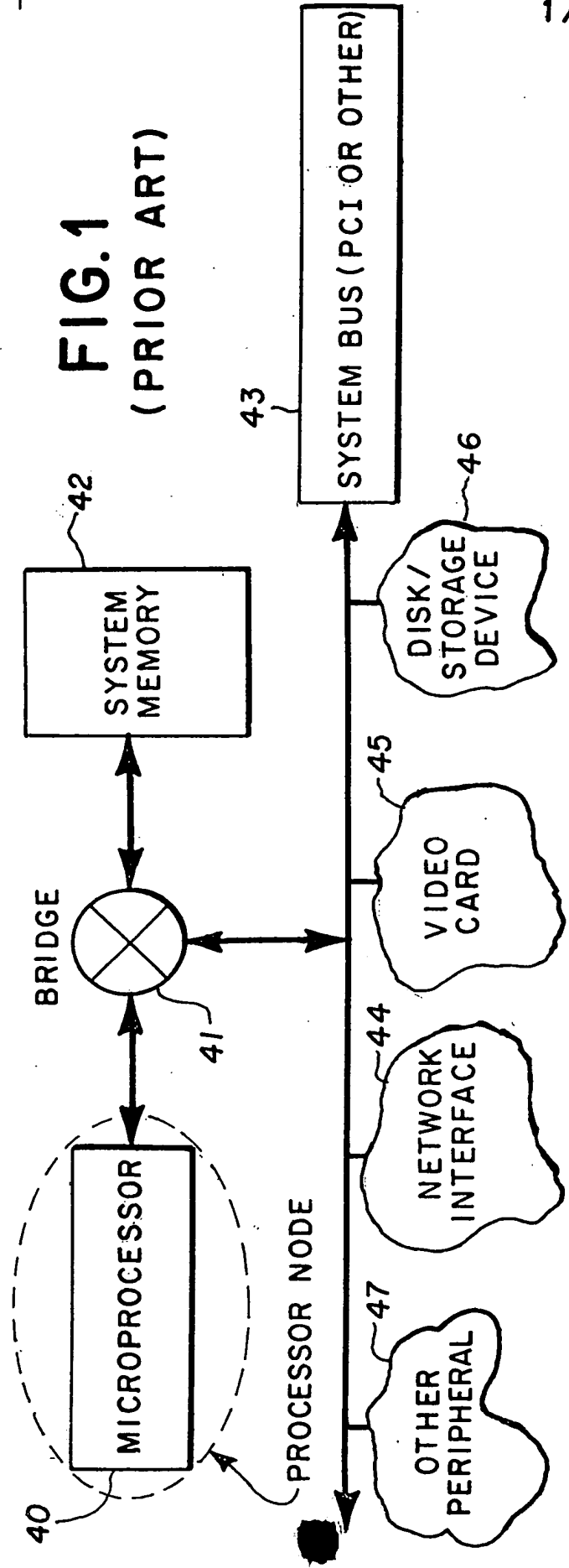
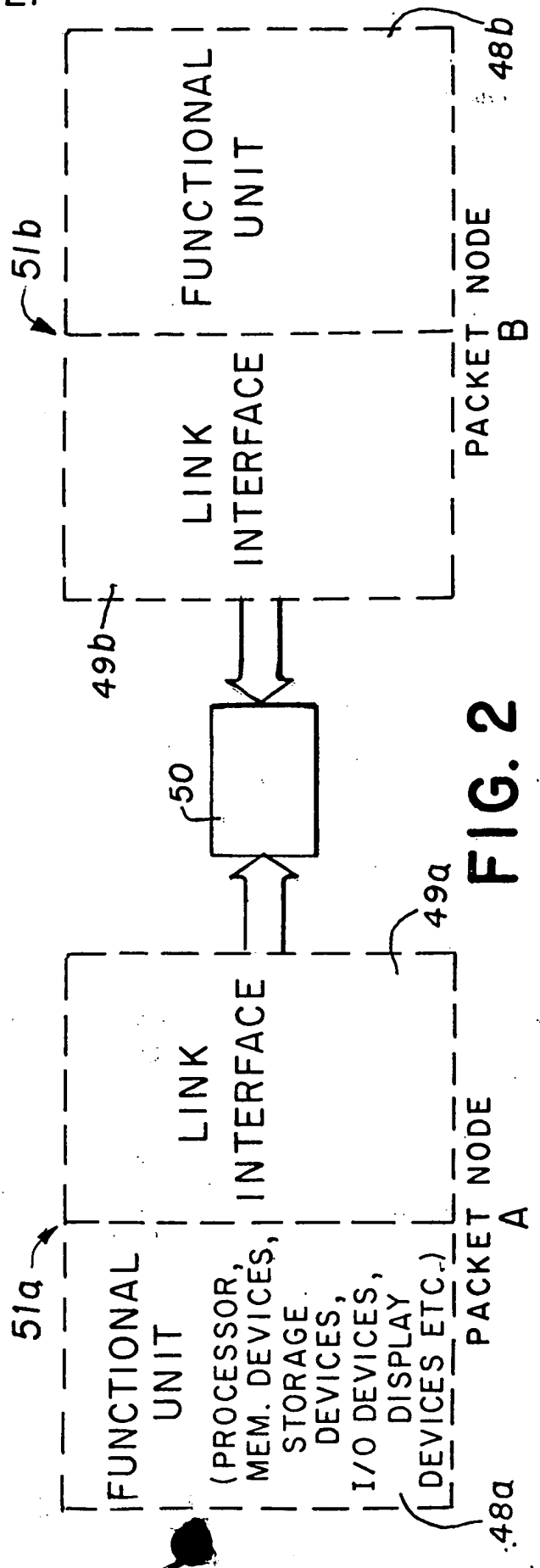


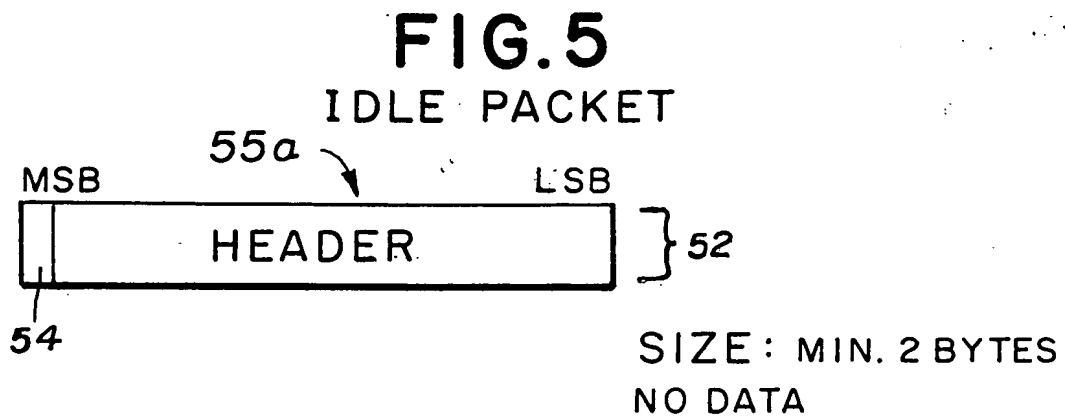
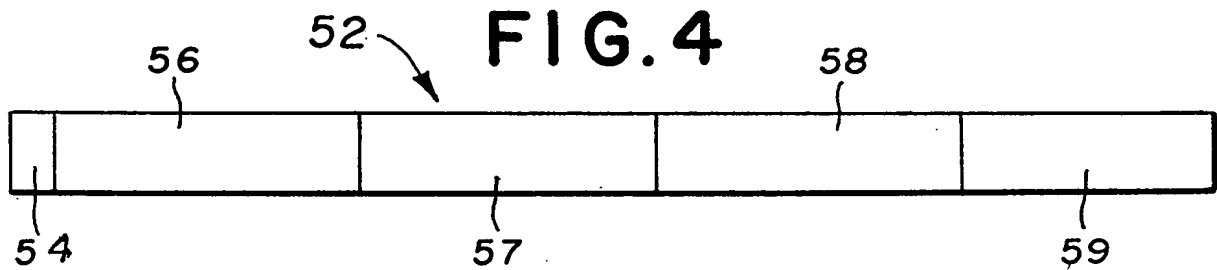
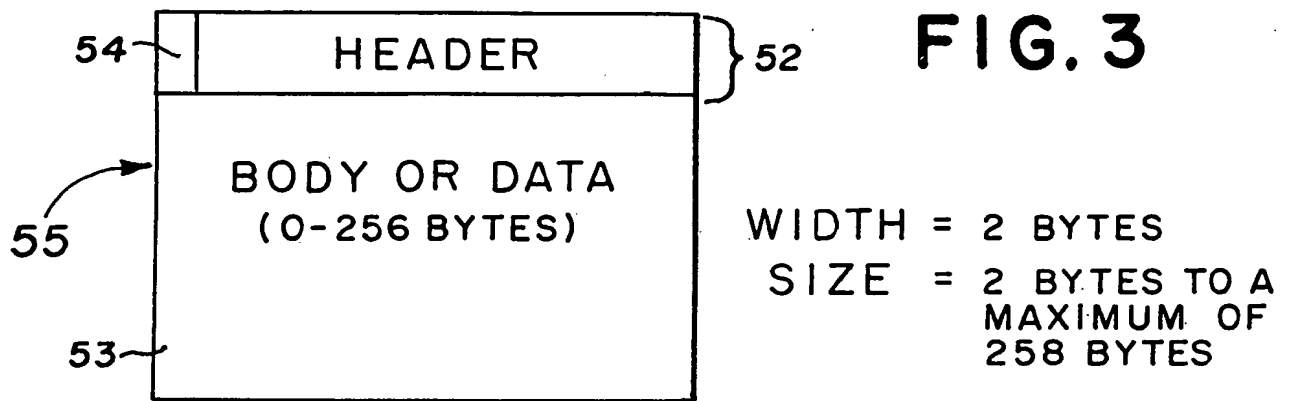
+

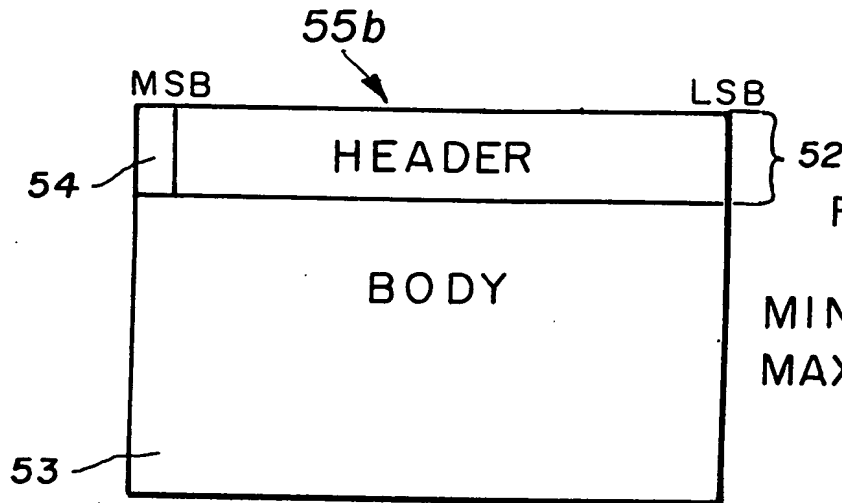


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+



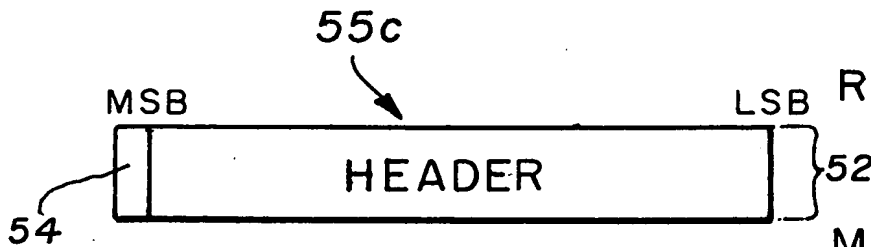


**FIG. 6**

REQUEST PACKET

MIN. SIZE: 4 BYTES

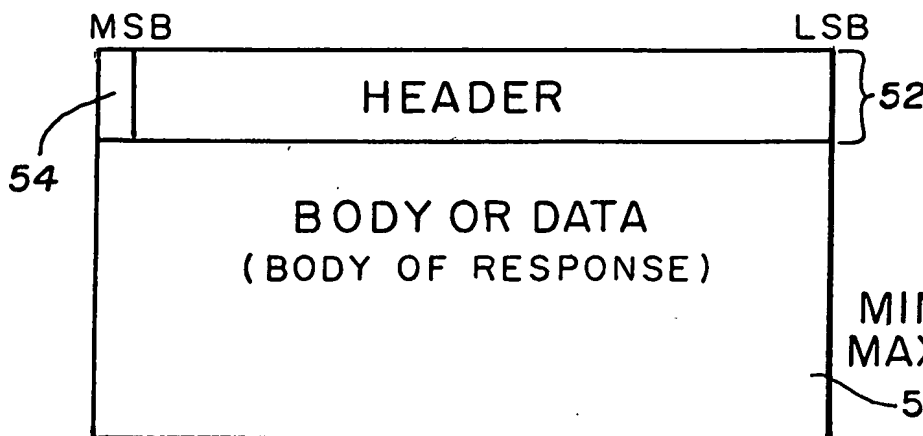
MAX. SIZE: 258 BYTES



**FIG. 7**

REQUEST ECHO  
PACKET

MIN. SIZE: 2 BYTES  
NO DATA OR BODY

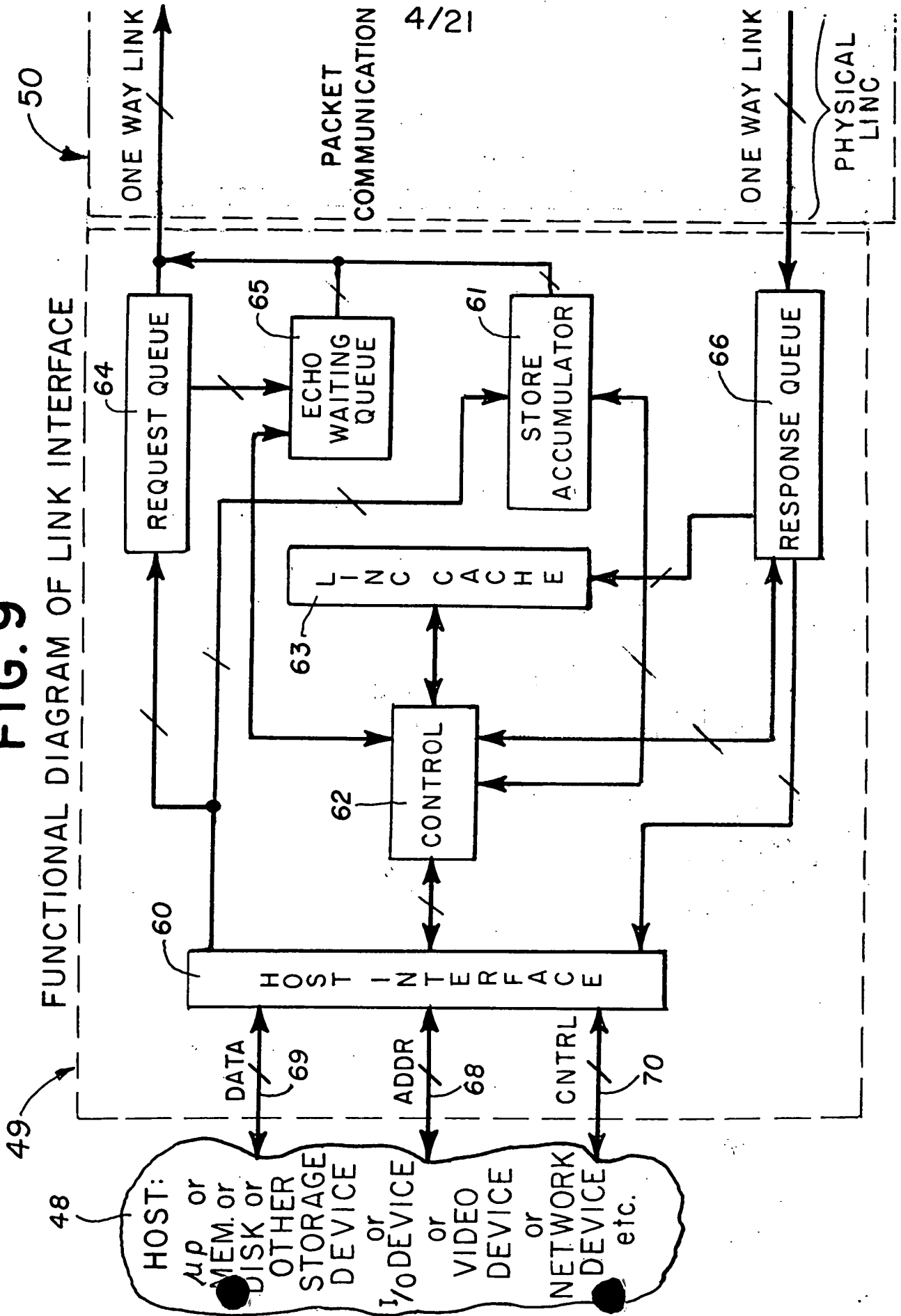


**FIG. 8**

RESPONSE  
PACKET

MIN. SIZE: 4 BYTES  
MAX. SIZE: 258 BYTES

# FIG. 9



+

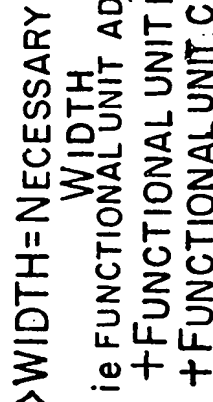
**LET**

**FIG. 10a**



DEPTH = n x MAXIMUM PACKET SIZE (258 BYTES) n=1,2,3...

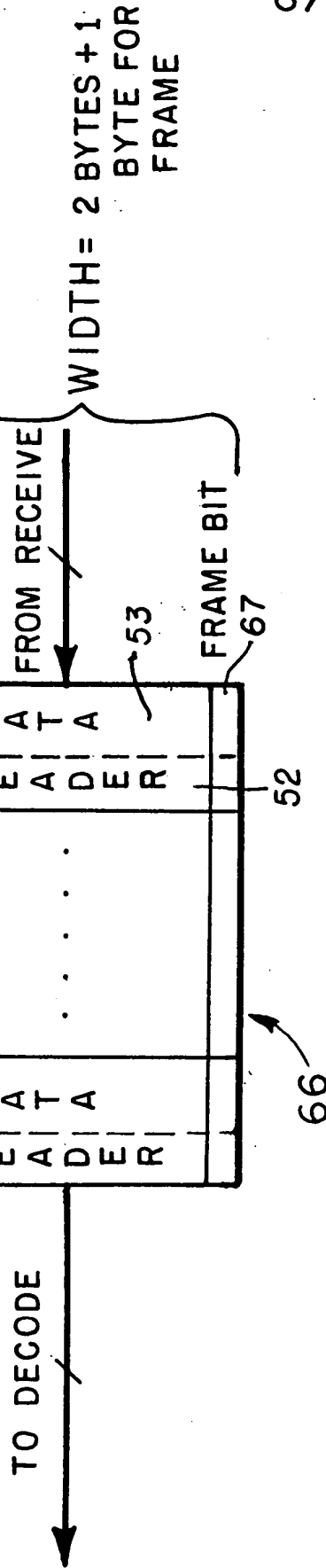
**FIG. 10b**



ie FUNCTIONAL UNIT ADDR.  
+FUNCTIONAL UNIT DATA  
+FUNCTIONAL UNIT CNTR

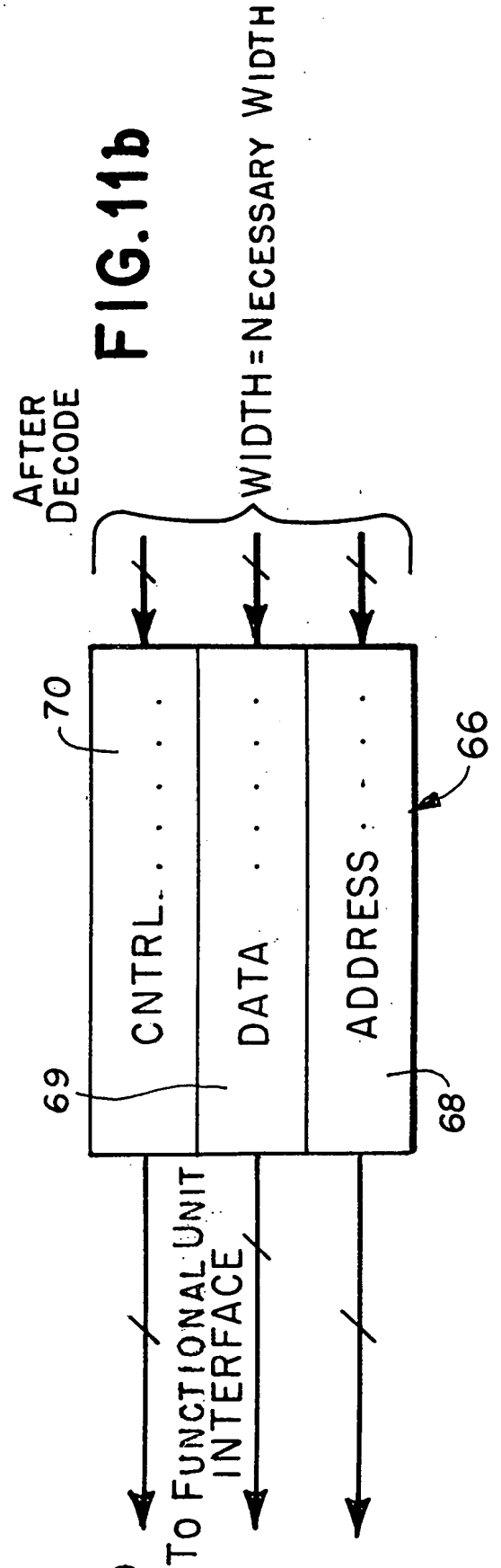
# POSSIBLE RESPONSE QUEUE STRUCTURES

FIG. 11a

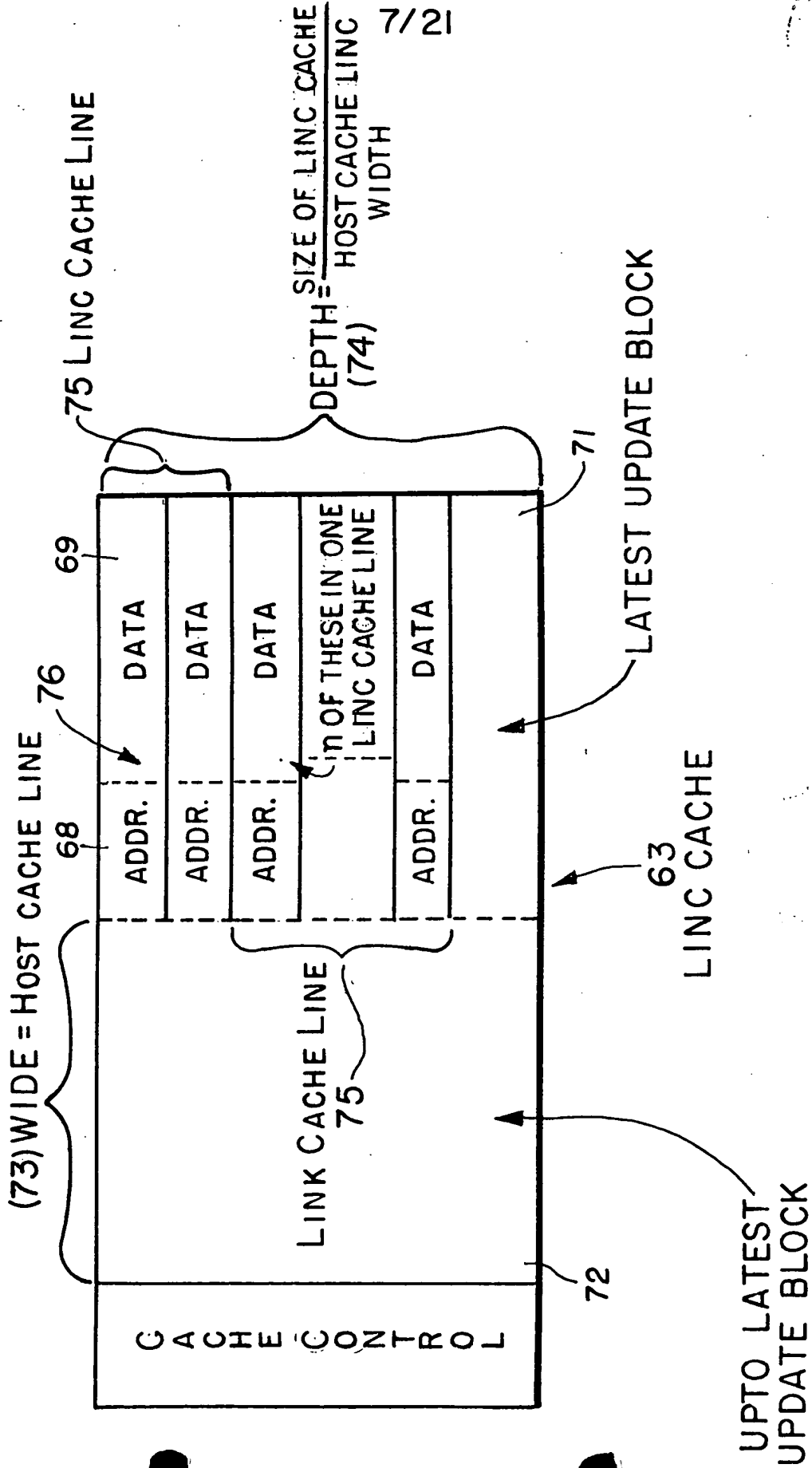


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FIG. 11b

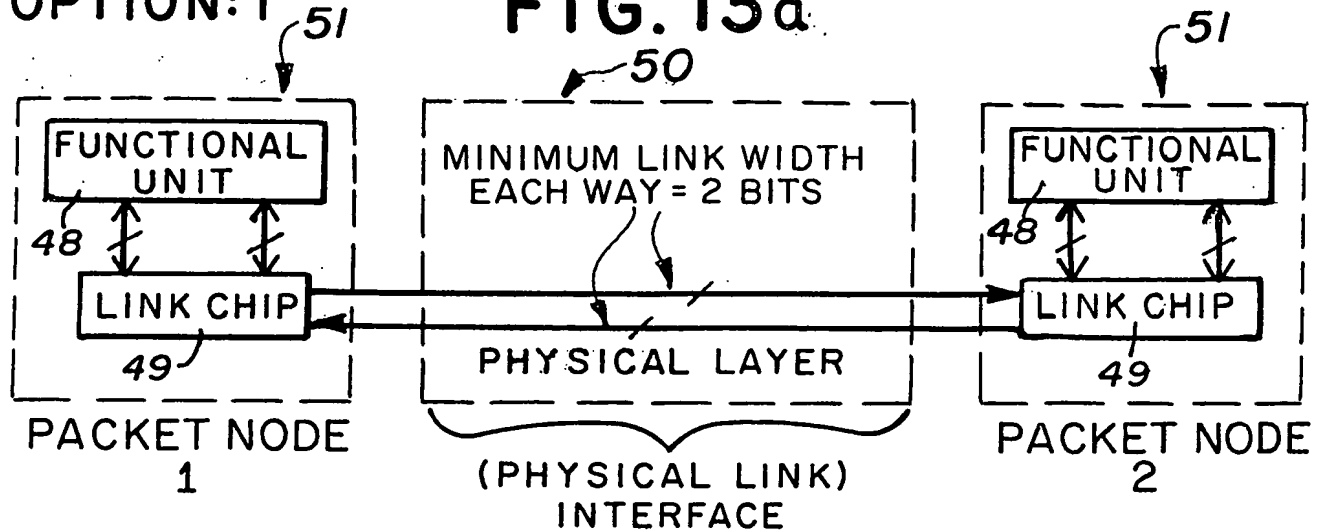


# FIG. 12



OPTION:1

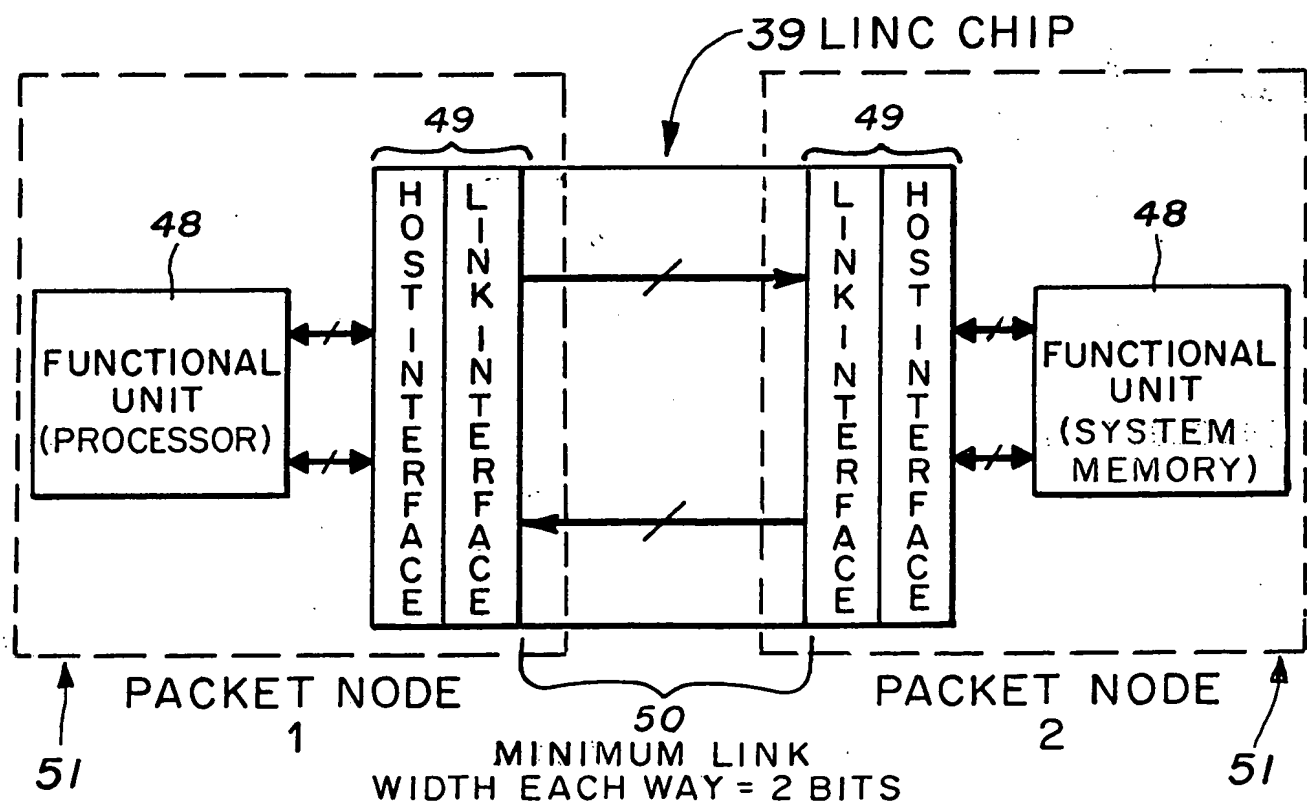
FIG. 13a



A SAMPLE TWO NODE LINK WHERE NODE 1 FUNCTIONAL UNIT IS THE PROCESSOR AND NODE 2 FUNCTIONAL UNIT IS THE MEMORY.

OPTION:2

FIG. 13b





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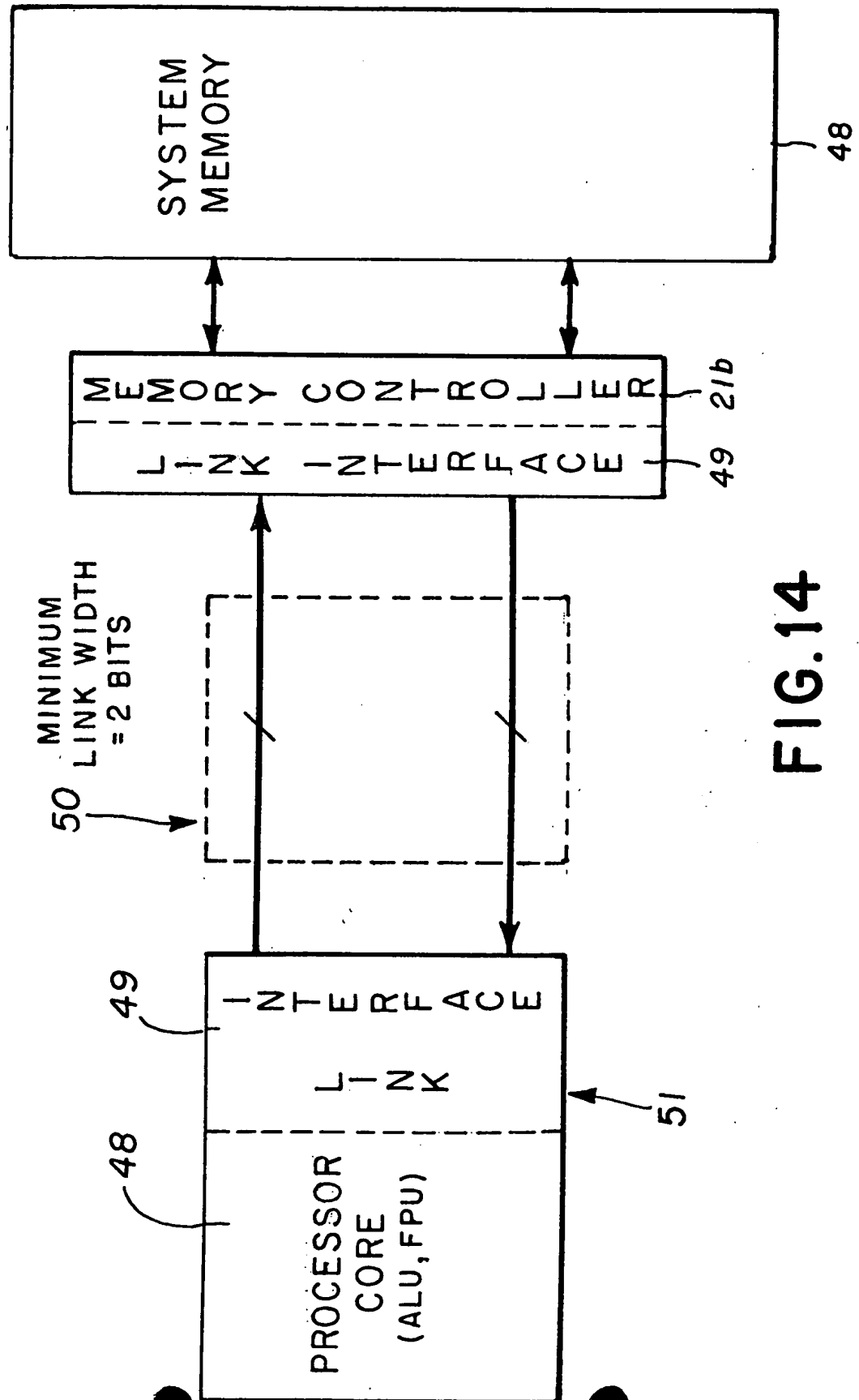
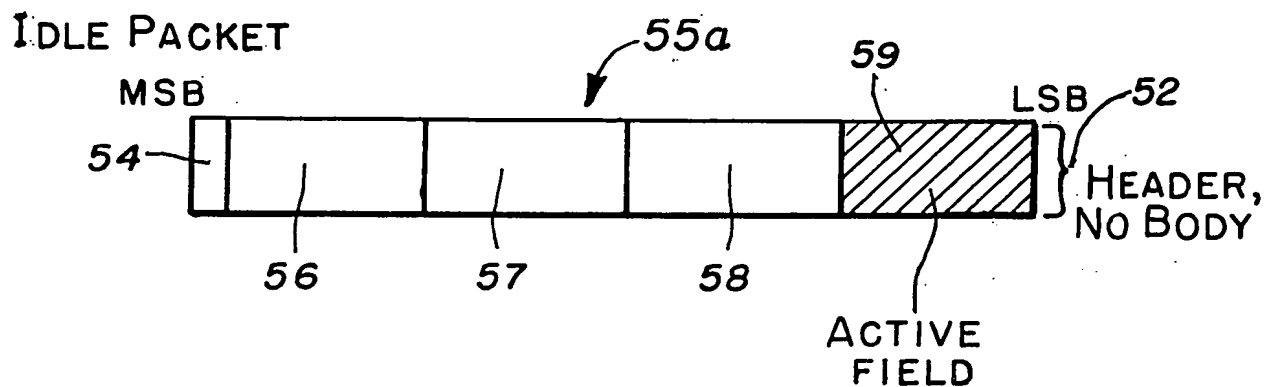
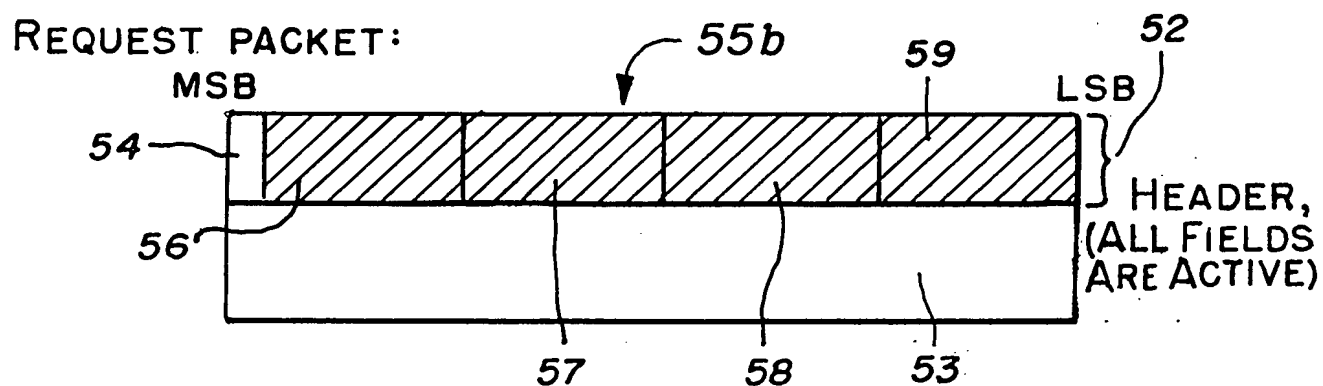
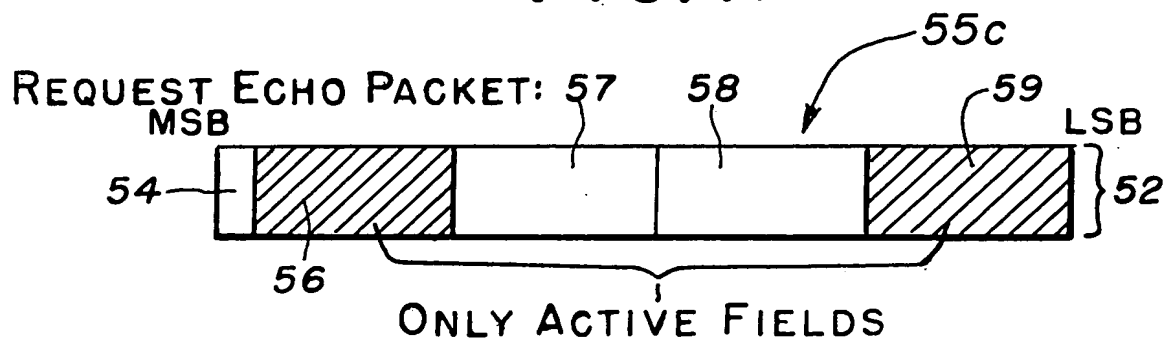


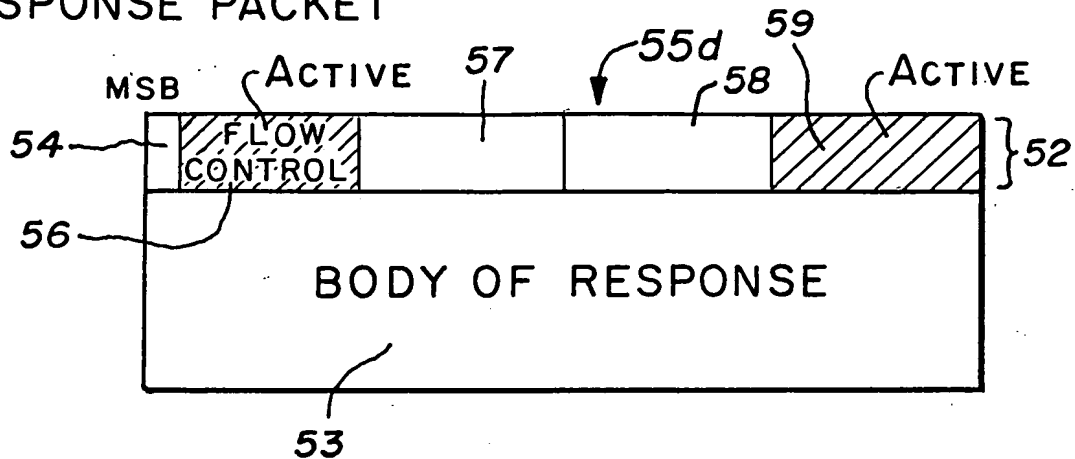
FIG.14

**FIG. 15****FIG. 16****FIG. 17**

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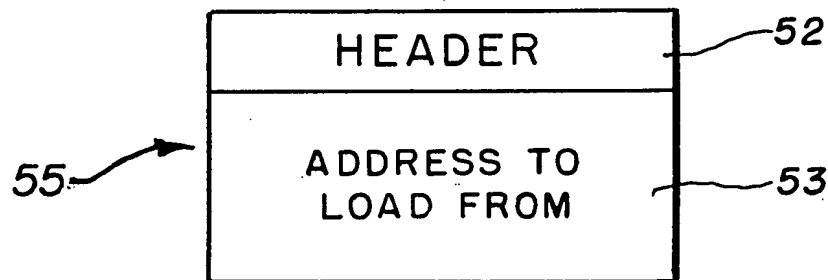
# FIG.18

RESPONSE PACKET

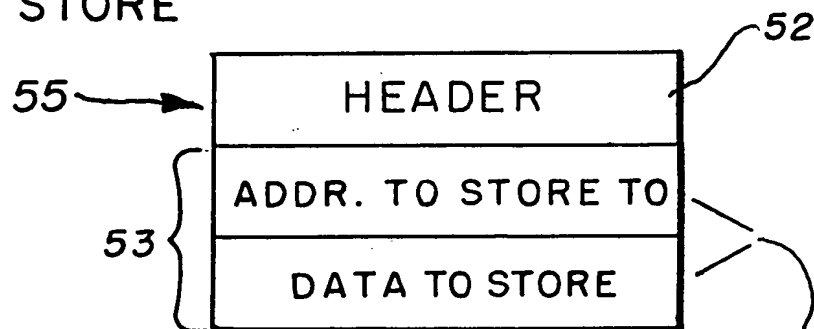


# FIG.19

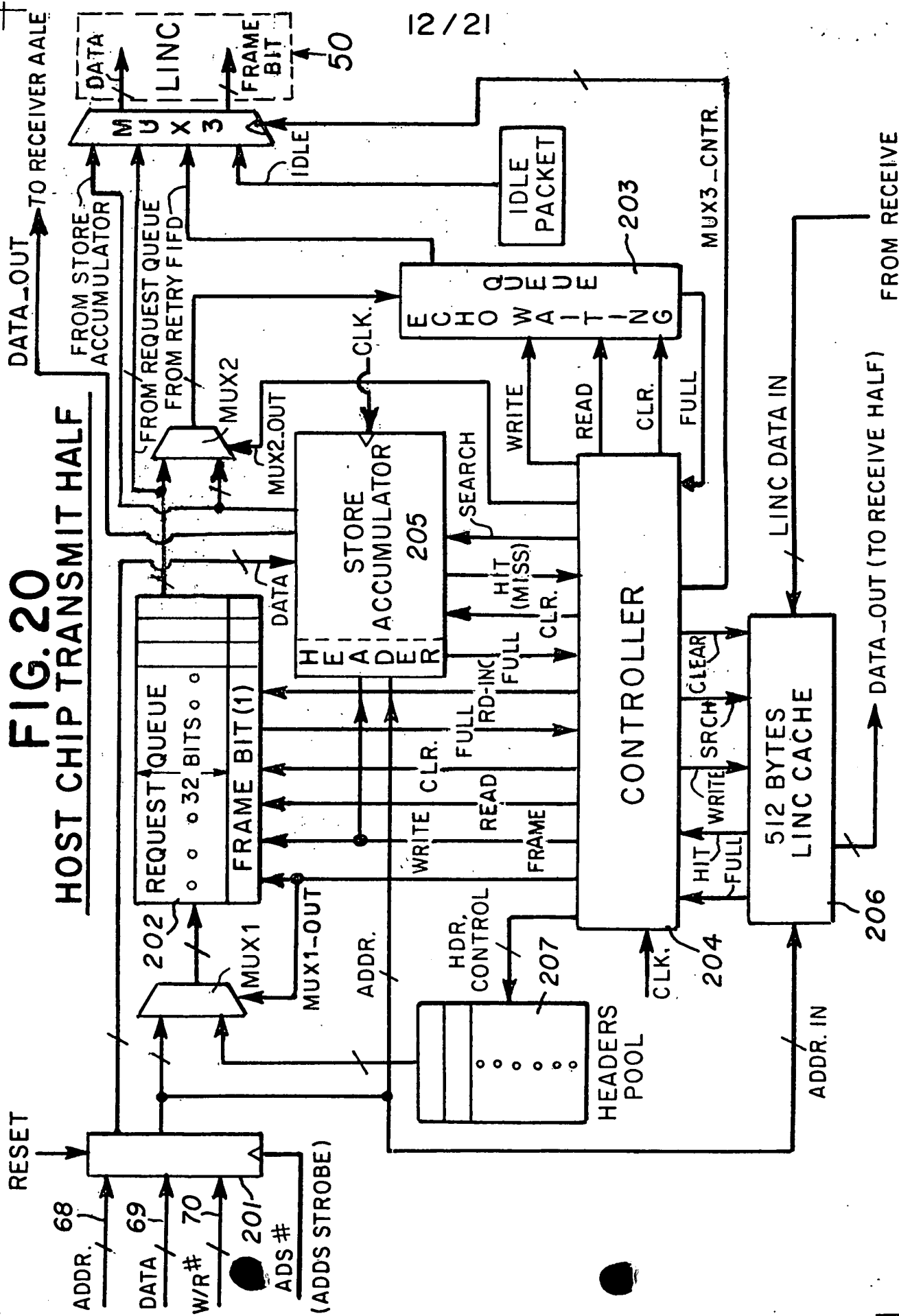
REQUEST PACKET  
FOR A LOAD



REQUEST PACKET  
FOR A STORE

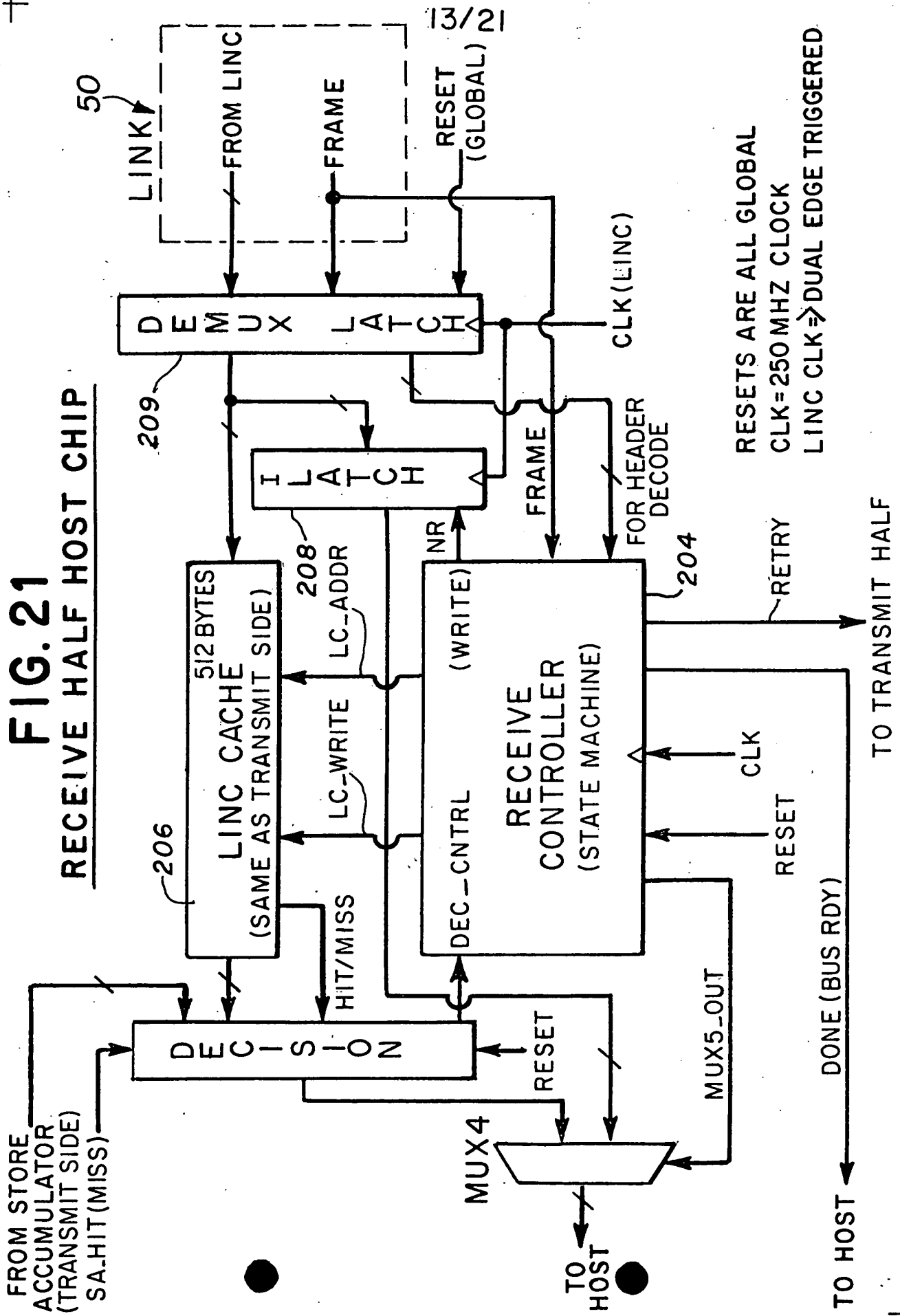


K OF EACH WHERE K IS  
THE NUMBER OF STORES  
IN THE STORE ACCUMU-  
LATOR.



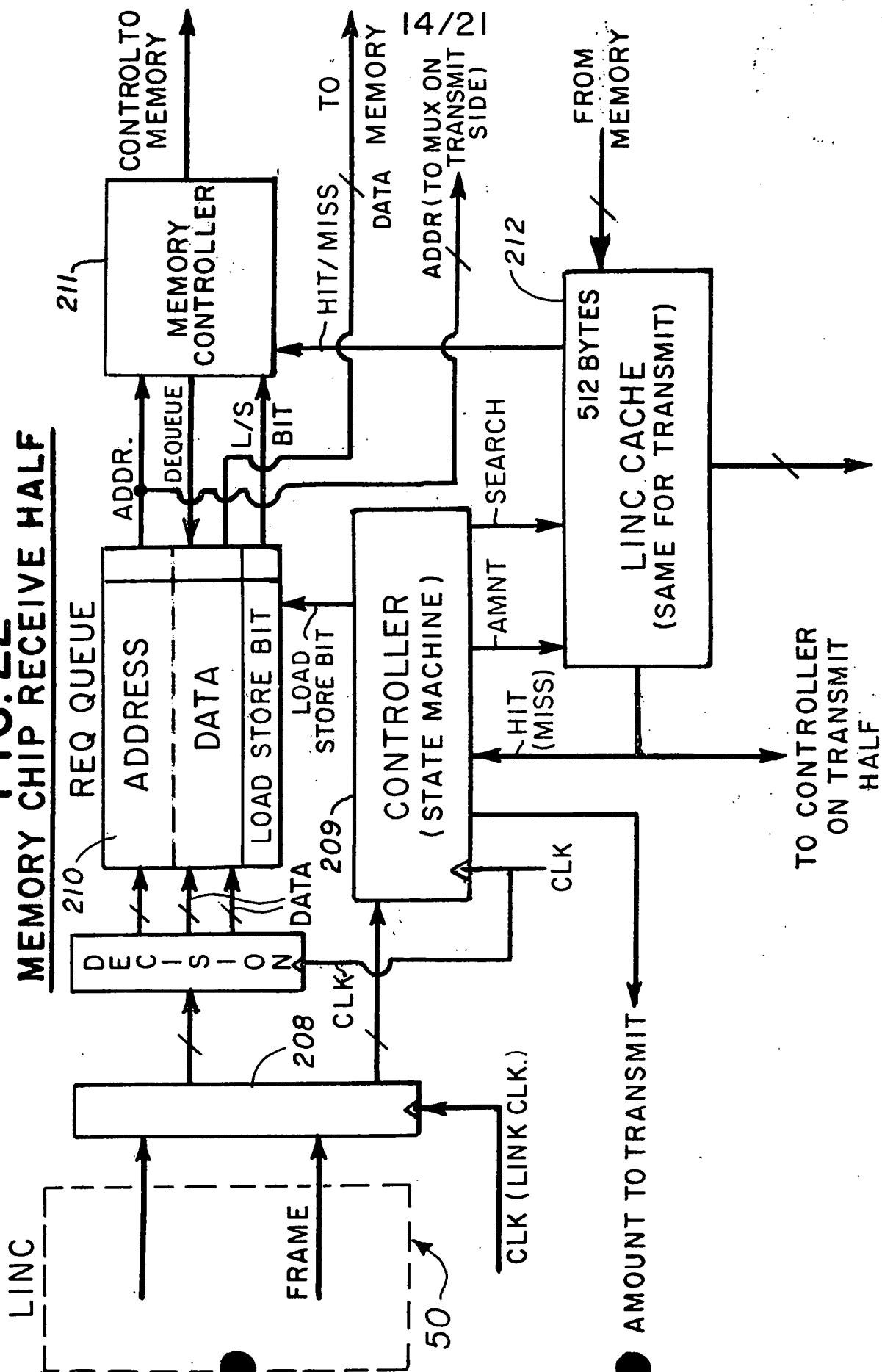
# FIG. 21

## RECEIVE HALF HOST CHIP



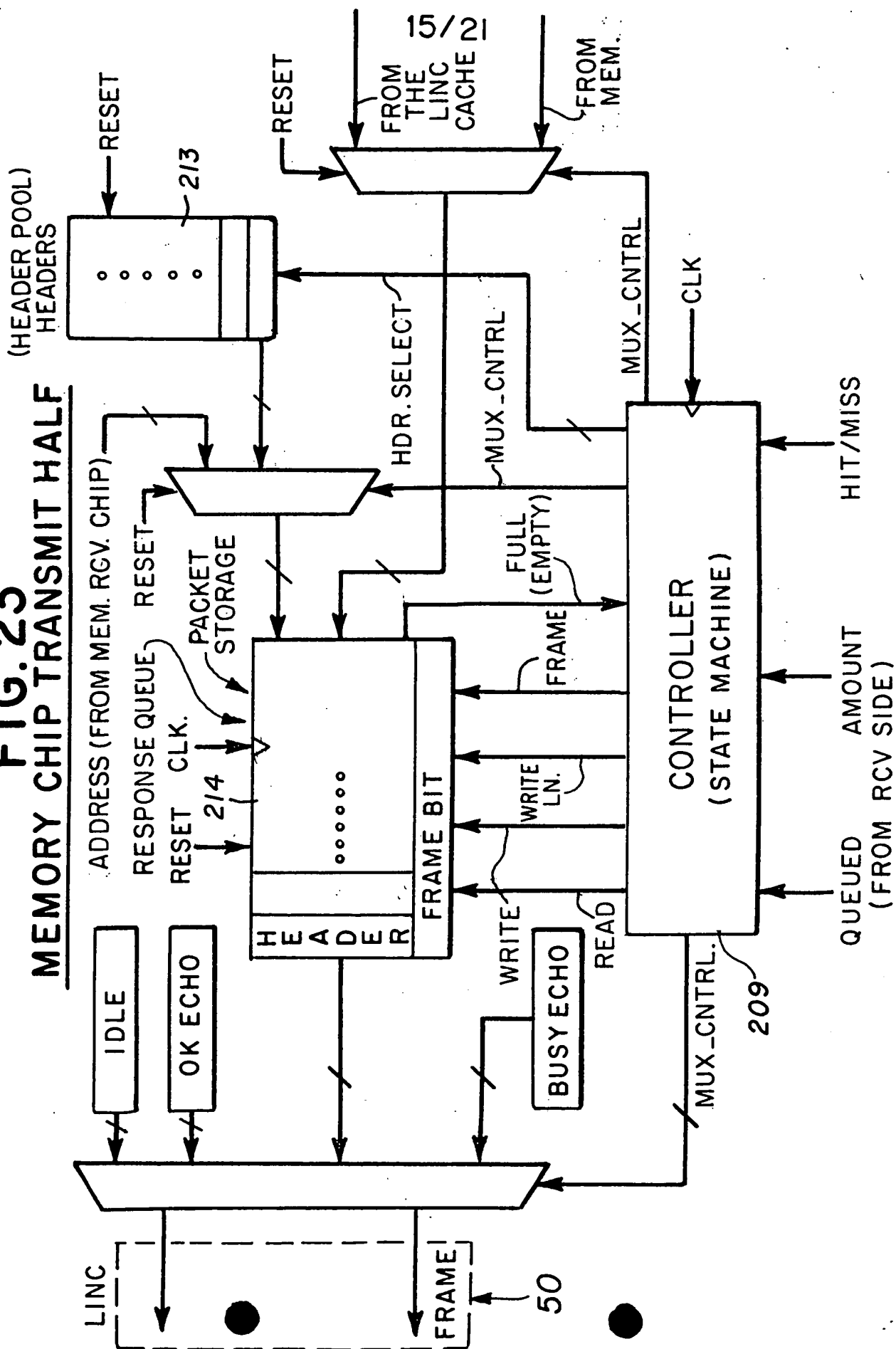
# FIG. 22

## MEMORY CHIP RECEIVE HALF



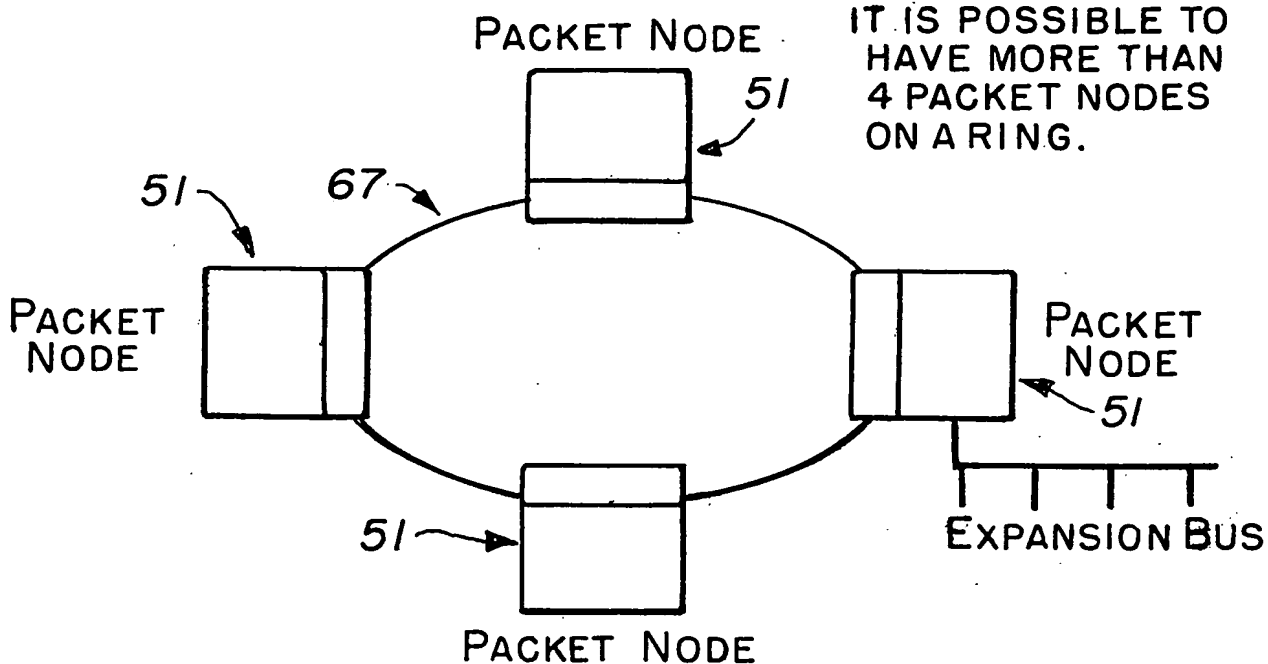
# FIG. 23

## MEMORY CHIP TRANSMIT HALF

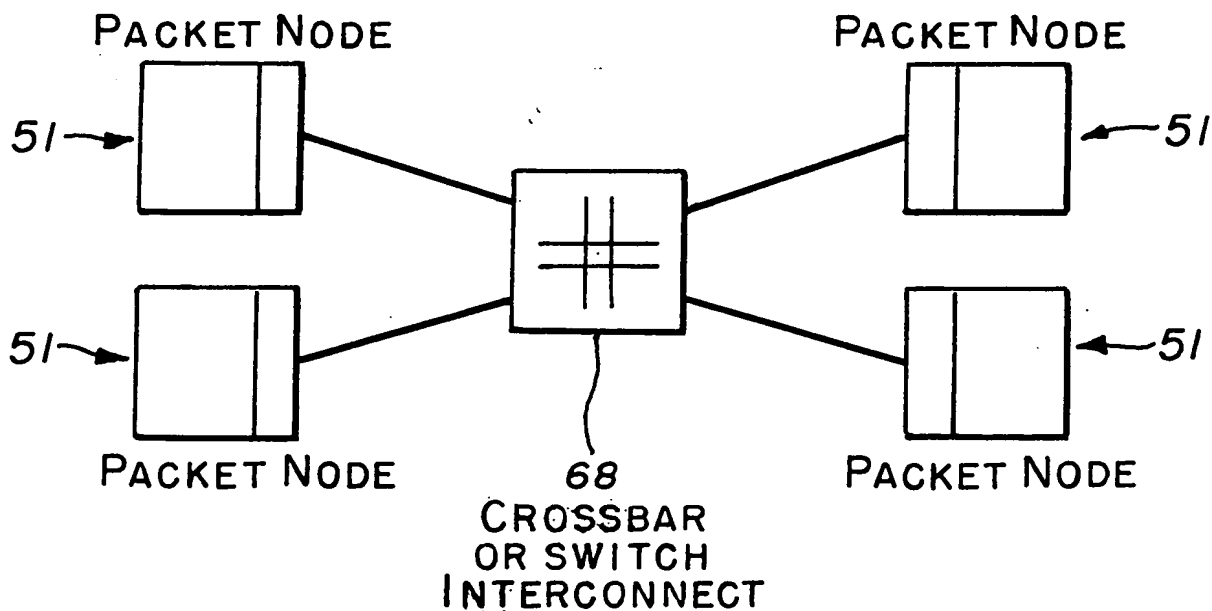


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**FIG. 24**



**FIG. 25**

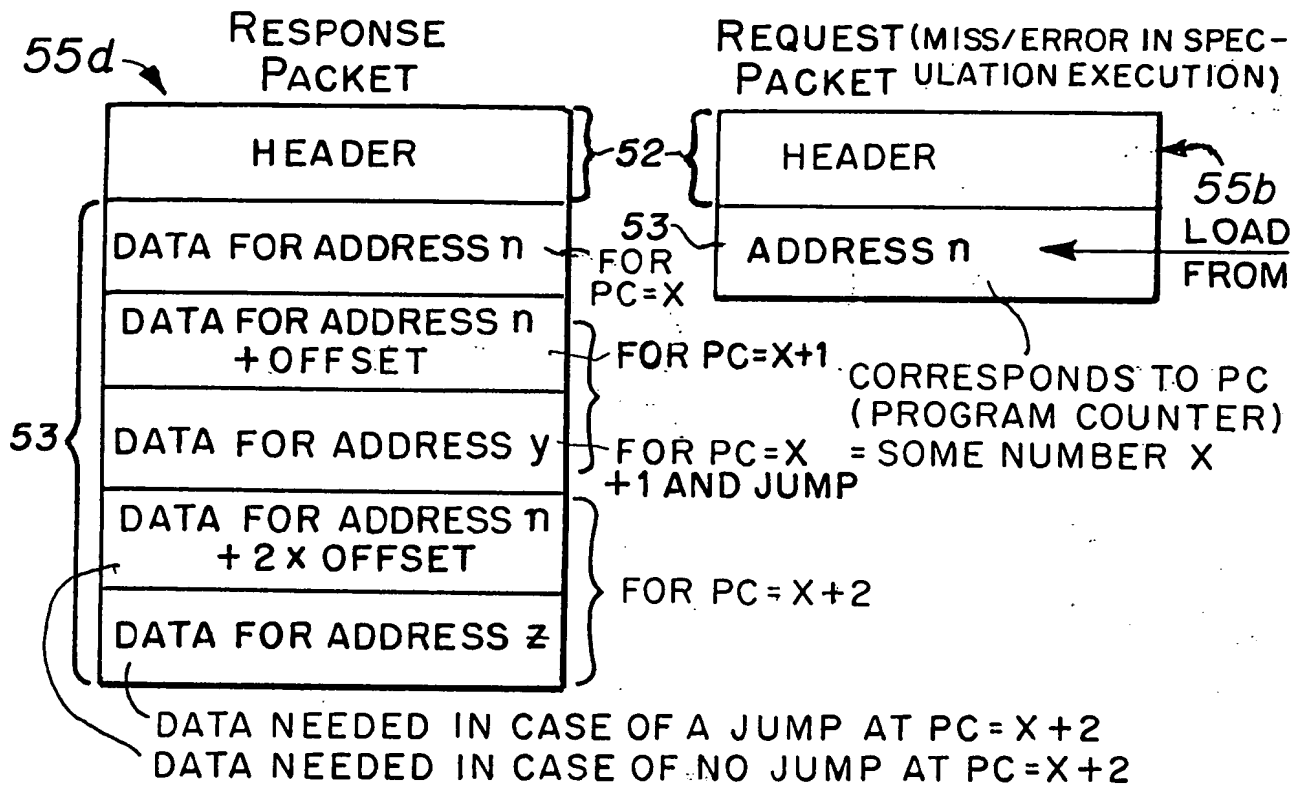




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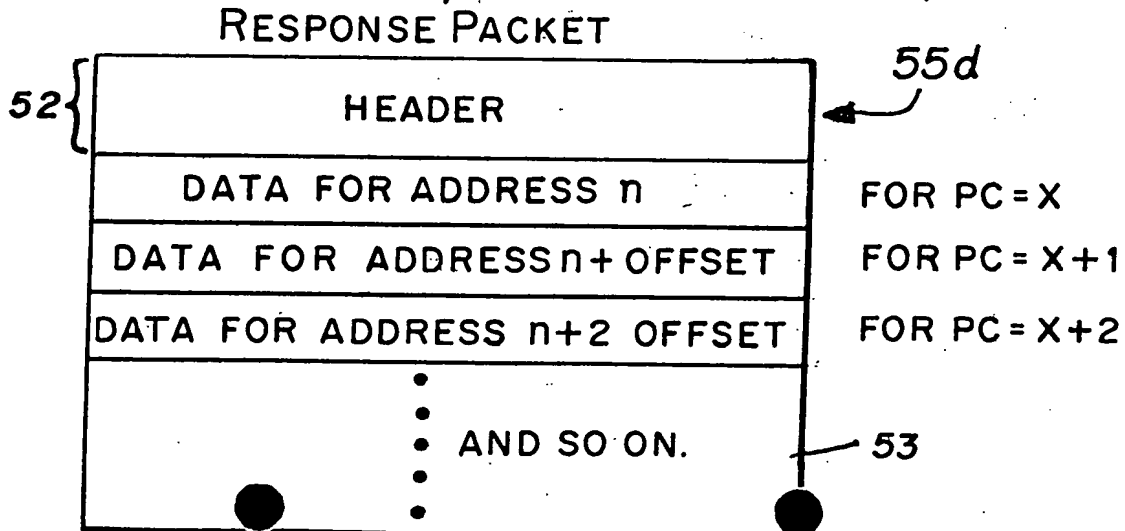
# FIG. 26

POSSIBLE RESPONSE PACKETS FOR A REQUEST  
WHEN ACCESS TO TLB AND OR BTB IN THE  
PROCESSOR IS AVAILABLE



AND SO ON.

FOR PROGRAMS WITH VERY HIGH LOCALITY  
(GRAPHICS, MULTIMEDIA ETC.)

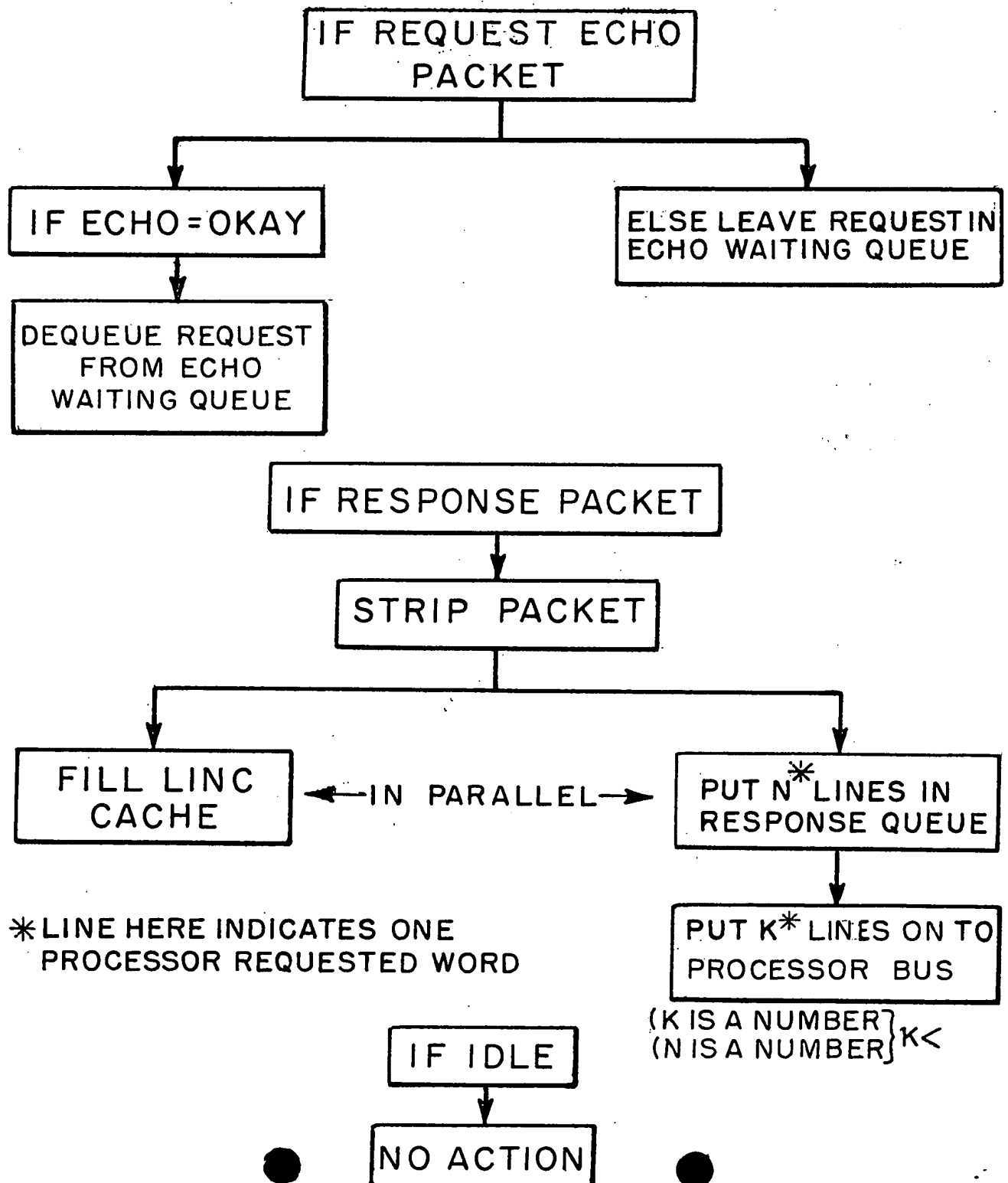


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## FIG. 27

### PROCESSOR NODE RECEIVE PROTOCOL

FOR PRESENT DETAILED IMPLEMENTATION, THE MEMORY NODE IS EXPECTED TO SEND ONLY THE FOLLOWING PACKETS.

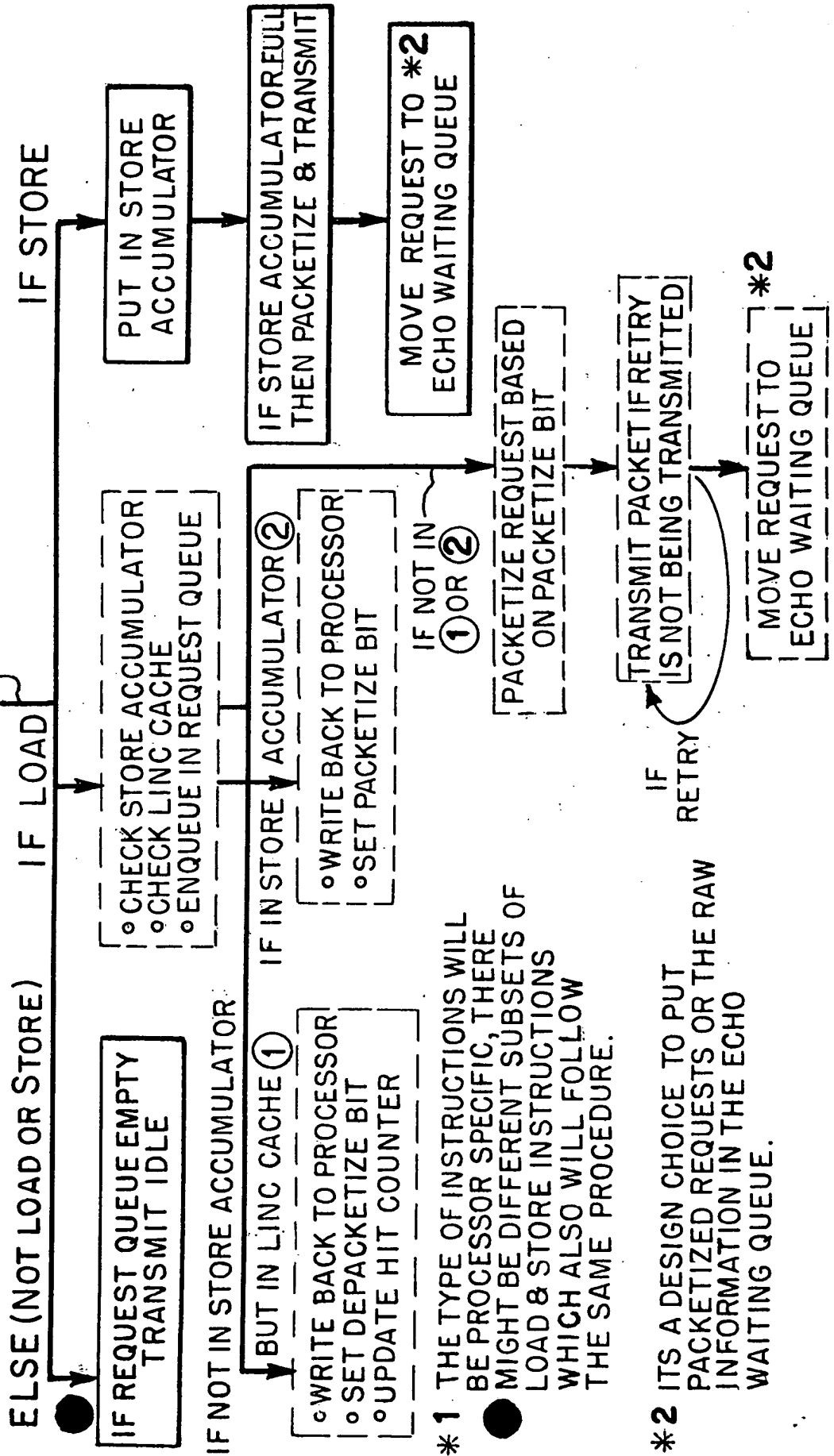


# FIG. 28

## PROCESSOR NODE TRANSMIT PROTOCOL

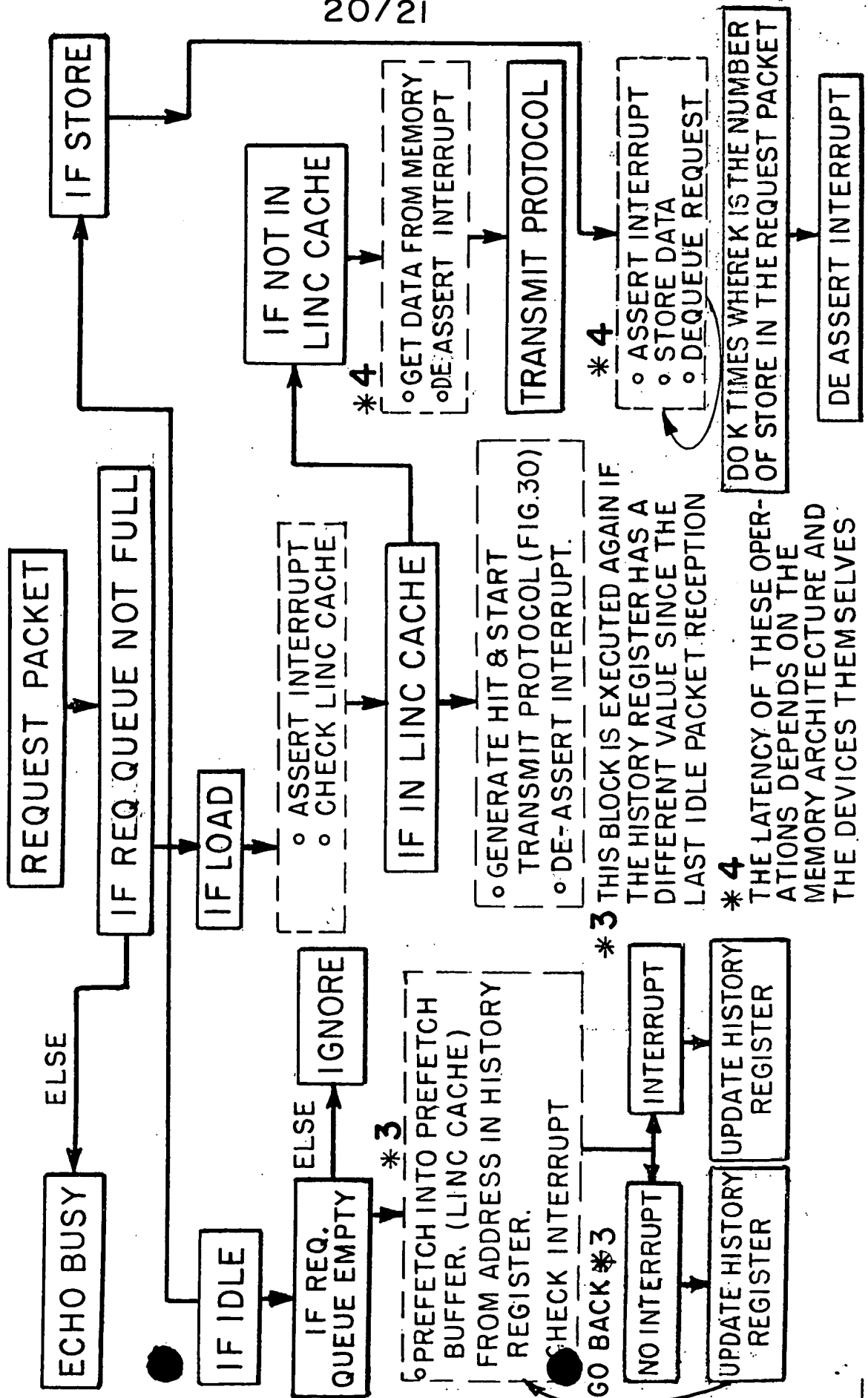
ALL ACTIONS WITHIN [ ] HAPPEN IN PARALLEL

CHECK LOAD OR STORE \*1



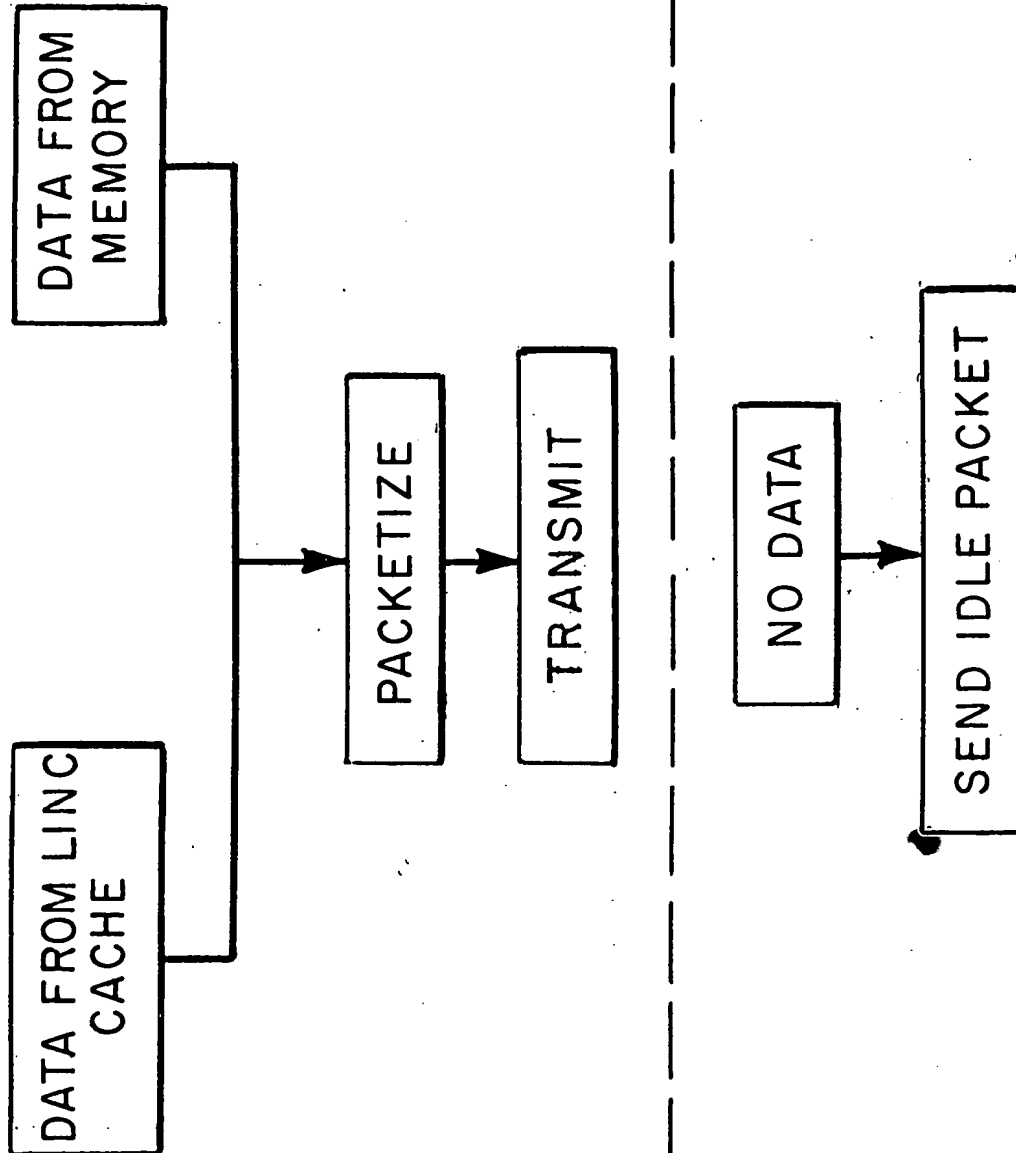
# FIG. 29

## MEMORY NODE RECEIVE PROTOCOL



+

**FIG. 30**  
**MEMORY NODE TRANSMIT PROTOCOL**



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